U-Band Receiver Modifications for Revision B

John B. Stephensen, KD6OZH

This document describes possible changes to the U-band receiver designed for AMSAT Eagle. The receiver will operate at a fixed frequency in the 435-438 MHz satellite segment in the 70-cm amateur band while in orbit, but the frequency needs to be set on the ground prior to launch. Since the receiver passband is 200 kHz wide, the frequency selection should be in 200 kHz or smaller increments.

There are two local oscillators (LOs) in the receiver. The first generates 634-637 MHz to mix with the RF input and generate and output at the first IF frequency of 199 MHz. The second must generate a constant frequency of either 188.3 MHz or 209.7 MHz to convert the output of the first IF amplifier to 10.7 MHz for further amplification and input to the SDX module.

In revision A, the frequency reference for the PLLs was either an on-board temperature-compensated crystal oscillator (TCXO) or an external reference as selected by the IHU via the CAN-DO widget. In revision B, this is replaced with one or two on-board crystal oscillators (PLXOs) that are phase-locked to the external reference.

There are 3 options for initializing the U-band receiver without IHU intervention. All use phase-locked loops (PLLs) with the differences being in what the PLLs control and how the PLLs are loaded with the constants that determine the output frequency.

1. Add PLXO and MCU to initialize current PLLs.
2. Add PLXO and change PLLs to a version that can be hard-wired.
3. Add 2 PLXOs and multiply outputs to final frequencies.

The following sections of this document describe these options. All exceed the phase-noise requirements documented at the beginning of this project.

The IHU remains responsible for monitoring the receiver via the CAN-DO widget. It can read the status of each PLL (locked or unlocked), measure the output voltage of the internal switching regulator and reset the MCU if it is present.

1. VCO-based Options

Two PLL options are presented using a common reference oscillator. In both cases, a PLL loop bandwidth is selected to minimize phase noise beyond 10 kHz offsets.

1.1 Common Phase-Locked Reference

The on-board PLXO must have low phase noise in order to maintain the accuracy of the external reference. A standard 10 MHz fundamental frequency AT-cut quartz crystal has the following characteristics.

Parameter	Value
F_O	10 MHz
ΔF	$\pm$10 PPM
C_O	6 pF
C_M	24 fF
X_M	667 kΩ
R_M	40 Ω

Figure 1 – 10 MHz Crystal Characteristics

The oscillator uses the crystal in a series-resonant mode and the output is taken via an amplifier in series with the crystal. This allows the crystal to lower the phase noise by filtering the output. The amplifier has a maximum noise figure of 5 dB and a 40-60 ohm input impedance. This noise figure may rise to 6 dB due to noise in the PLL. The crystal operates with a 100 μW dissipation to maintain stability in a free-running mode and the output amplifier collects at least this amount of power from the oscillator. The broad band noise floor is then -174 + 6 + 10 or -158 dBc/Hz.

The minimum loaded Q of the crystal is 6667 when the input impedance of the amplifier is 60 ohms, resulting in a 1.5 kHz bandwidth. Since the flicker corner is at least 5 kHz, the oscillator noise rises at 30 dB per octave inside the resonator bandwidth. The estimated phase noise is shown in figure 2, below.

Offset (Hz)	Noise (dBc/Hz)
750	-158
100	-132
10	-102

Figure 2 – Low-Noise 10 MHz Phase-Locked Oscillator Characteristics

If the external reference disappears or goes off frequency, the PLXO will stay within $\pm$20 PPM of the correct frequency. This may cause the receiver to be off frequency by as much as 9 kHz.

1.2 MCU Initialization of Integer-N PLLs

In this approach, a microcontroller unit (MCU) with flash memory is added to the current PCB. The frequency is determined by a set of values stored in the flash memory of the MCU. The values are part of the program code loaded via a connector accessing the 3-wire programming interface to the MCU. The MCU configures the PLLs when power is applied or when reset via the CAN-DO bus.

The flash memory must have the highest possible reliability and the leakage of EEPROM and flash memory increases exponentially with temperature. MCU selection was based on the availability of a high operating temperature version and a long data retention time. The PIC16F506-E MCU has 1024 words of program memory, 67 bytes of data memory, retains data for more than 40 years and operates over a –40 to +125 C temperature range. This MCU comes in a 14-pin SOIC package and has 12 I/O pins. Three pins are brought out to the programming connector, five are used to configure the two PLLs and one is used to enable a test mode. There are three unused pins.

The PLL is configured for 200 kHz channels by dividing the reference by 50. The following graph shows the expected phase noise of the first LO in dBc/Hz over 6 decades of frequency offset.

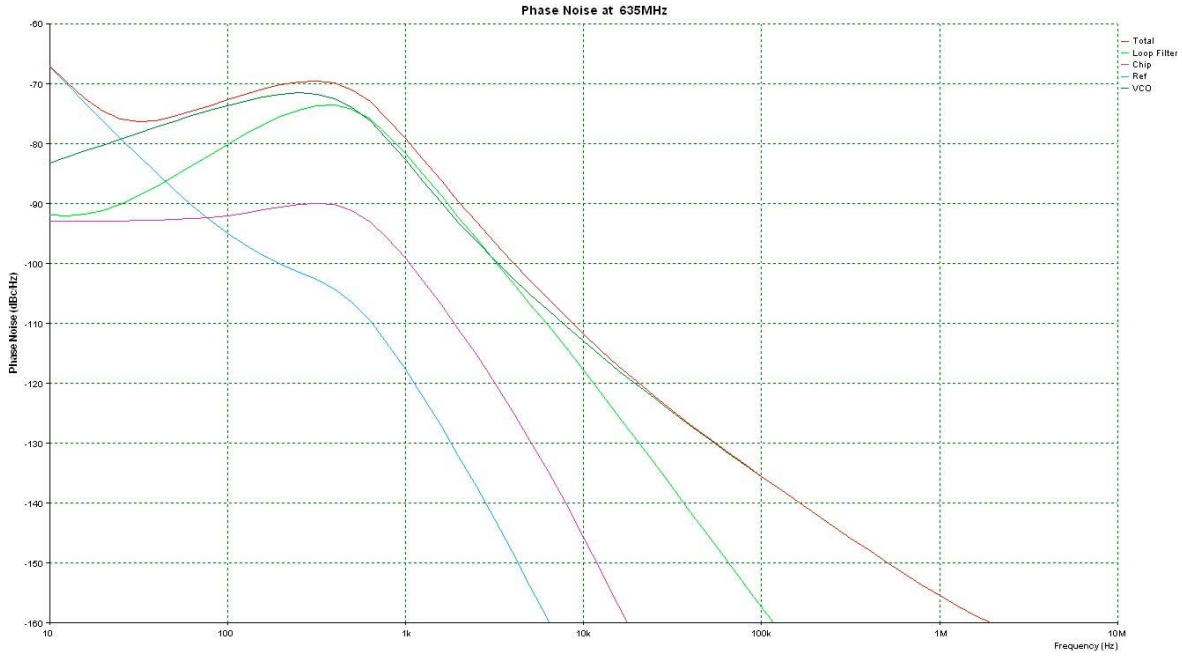

Figure 3 – Expected Phase Noise of Integer-N PLL

1.3 Hard-Wired Delta-Sigma PLLs

In this approach, a set of zero-ohm resistors is installed on the PCB to set the frequency. A test point would allow fast frequency shifts for testing.

The PLLs are currently PE3238 (commercial) or PE9702 (radiation-hardened) integer-N devices in a 44-pin PLCC or CQFJ package. This integer-N PLL requires that the phase detector frequency is the same as the channel spacing and the small number of external pins precludes hard-wiring the frequency. These could be replaced with PE9763 or PE97632 delta-sigma PLLs in a 68-pin CQFJ package. The delta-sigma modulator allows the phase detector frequency to be increased to 10 MHz without increasing channel spacing and the extra pins allow programming in 40 Hz increments. The PE9763 draws 5 mA more DC current than the current PLL and is only available in a radiation-hardened version.

The following graphs show the expected phase noise of the first LO in dBc/Hz over 6 decades of frequency offset. The delta-sigma PLL allows more choices in loop bandwidth so two examples are shown.

Figure 4 shows the phase noise with the loop bandwidth optimized to minimize phase noise above 10 kHz offsets. It also improves phase noise over that of the integer-N PLL by up to 10 dB between 20 Hz and 1 kHz offsets.

Figure 5 shows the phase noise with the loop bandwidth optimized to minimize phase noise below 5 kHz offsets. This version improves phase noise over the integer-N PLL by up to 34 dB between 20 Hz and 5 kHz offsets at the cost of increasing phase noise by up to 10 dB between 5 kHz and 100 kHz offsets.

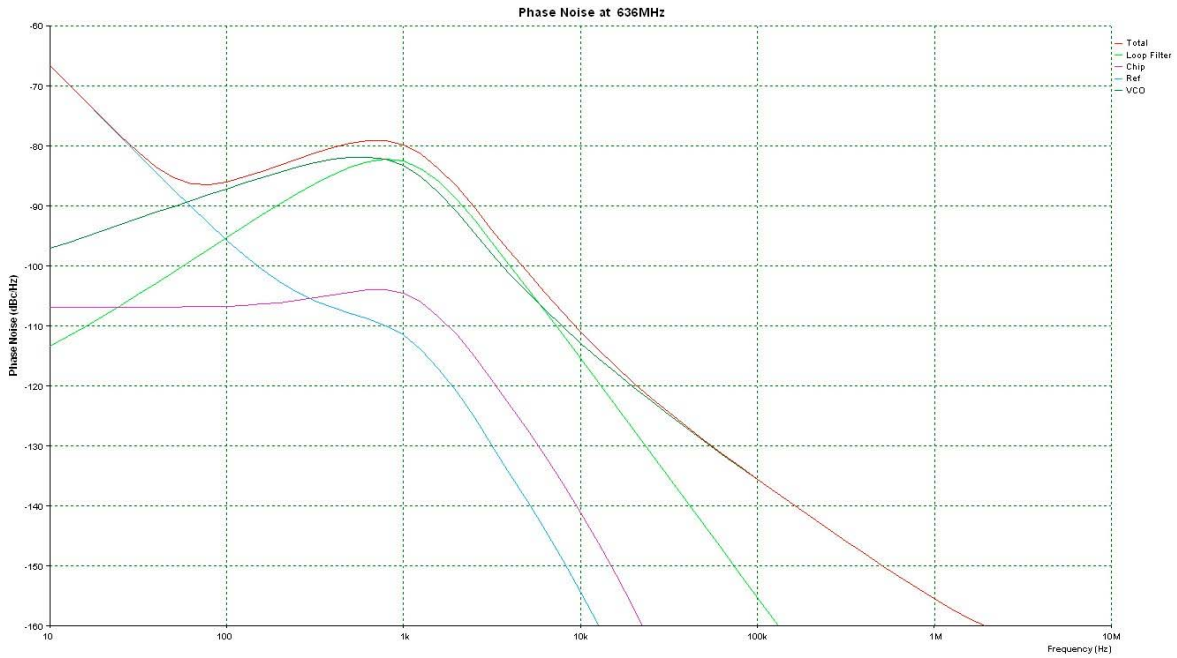

Figure 4 – Expected Phase Noise of Delta-Sigma PLL (Narrow Loop Bandwidth)

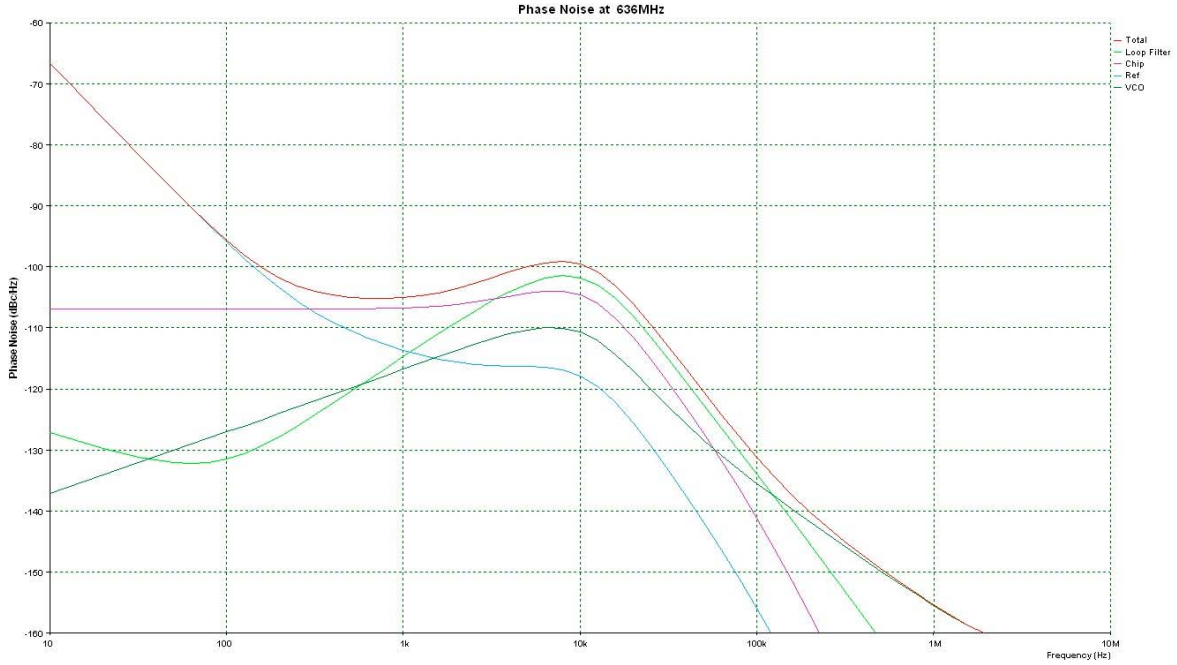

Figure 5 – Expected Phase Noise of Delta-Sigma PLL (Wide Loop Bandwidth)

2. Oscillator/Multiplier Option

In this approach, two VCXOs are used to set the frequency of the receiver and each is locked to the external reference. The complexity of each PLL is the same for a VCO or VCXO -- the frequency is just lower. The PLLs could be integer-N or delta-sigma types. If a channel spacing of 125 kHz or more is satisfactory, integer-N PLLs can be used with a MCU to set the frequency. If finer frequency control is required or the frequency must be hard-wired, delta-sigma PLLs can be used.

The VCXO crystals are custom-made with one at a predetermined frequency and one at a frequency related to the final operating frequency. Crystals operating on the 5th, 7th or 9th overtone at 100-160 MHz are used. The output of the second VCXO is multiplied by a factor of 2 to generate 188.3 or 209.7 MHz. The output of the first VCXO is multiplied by a factor of 4, 5 or 6 to generate a 634-637 MHz output.

Depending on the frequency multiplication scheme, various spurious products are generated in the receiver when the fundamental and harmonics of the crystal oscillator mix with the fundamental and harmonics of the RF input. Unfortunately, there are one or more spurious products at PAVE PAWS frequencies for all possible designs. These spurs can be attenuated by careful filtering in the oscillator/multiplier chain, but the additional complexity decreases reliability and they cannot be completely eliminated.

LO	RF	--Fmin--	--Fmax--	LO	RF	--Fmin--	--Fmax--	LO	RF	--Fmin--	--Fmax--
4	1	435.000	438.000	4	2	416.500	418.000	6	3	383.333	384.833
7	2	455.250	457.875	7	3	436.167	437.917	8	3	489.000	491.000
9	3	409.167	411.417	10	3	462.000	464.500				

Figure 6 – Spurious Response Table for Quadrupler

LO	RF	--Fmin--	--Fmax--	LO	RF	--Fmin--	--Fmax--	LO	RF	--Fmin--	--Fmax--
2	1	452.600	453.800	5	1	435.000	438.000	5	2	416.500	418.000
6	2	479.900	481.700	8	2	407.700	410.100	8	3	404.467	406.067
9	2	471.100	473.800	9	3	446.733	448.533	10	3	489.000	491.000

Figure 7 – Spurious Response Table for Quintupler

LO	RF	--Fmin--	--Fmax--	LO	RF	--Fmin--	--Fmax--	LO	RF	--Fmin--	--Fmax--
2	1	410.334	411.334	6	1	435.002	438.002	6	2	416.501	418.001
7	2	469.335	471.085	9	3	383.334	384.834	10	2	428.835	431.335
10	3	418.557	420.223								

Figure 8 – Spurious Response Table for Sextupler

All quadrupler spurs within the 420-250 MHz range used by PAVE PAWS are in the amateur satellite segment, so this is the best option.

Low phase noise VCXOs maintain the accuracy of the external reference. Standard 5th overtone 106 MHz AT-cut quartz crystals have the following characteristics.

Parameter	Value
F_O	106 MHz
ΔF	$\pm$10 PPM
Overtone	5^{th}
C_O	6 pF
C_M	1 fF
X_M	1.5 MΩ
R_M	60 Ω

Figure 9 – 106 MHz Crystal Characteristics

The oscillator uses the crystal in a series-resonant mode and the output is taken via an amplifier in series with the crystal. This allows the crystal to lower the phase noise by filtering the output. The amplifier has a maximum noise figure of 5 dB and a 40-60 ohm input impedance. This noise figure may rise to 6 dB due to noise in the PLL. The crystal operates with a 100 μW dissipation to maintain stability in a free-running mode and the output amplifier collects a minimum of 63 μW from the oscillator. The broad band noise floor is then -174 + 6 + 12 or -156 dBc/Hz.

The minimum loaded Q of the crystal is 12,500 when the input impedance of the amplifier is 60 ohms, resulting in an 8.2 kHz bandwidth. Since the flicker corner is at least 5 kHz, the oscillator noise rises at 30 dB per octave inside the resonator bandwidth. The estimated phase noise is shown in figure 2, below.

Offset (Hz)	Noise (dBc/Hz)
4000	-156
1000	-138
100	-108
10	-78

Figure 10 – Low-Noise 106 MHz Phase-Locked Oscillator Characteristics

The crystal oscillator/multiplier has a higher phase noise floor due to a lower resonator power level and the 6-7 dB per octave increase with multiplication. The multipliers increase the phase noise by 18 dB and 7 dB for the first and second LOs.

Offset (Hz)	Crystal (dBc/Hz)	LO1 (dBc/Hz)	LO2 (dBc/Hz)
4000	-156	-138	-149
1000	-138	-120	-131
100	-108	-90	-101
10	-78	-60	-71

Figure 11 – Estimated VCXO/Multiplier Phase Noise

Phase noise from the first LO dominates the receiver so it is the most critical. Figure 11 shows the phase noise of the outputs and figure 12 compares the first LO phase noise for the VCXO/multiplier and VCO schemes.

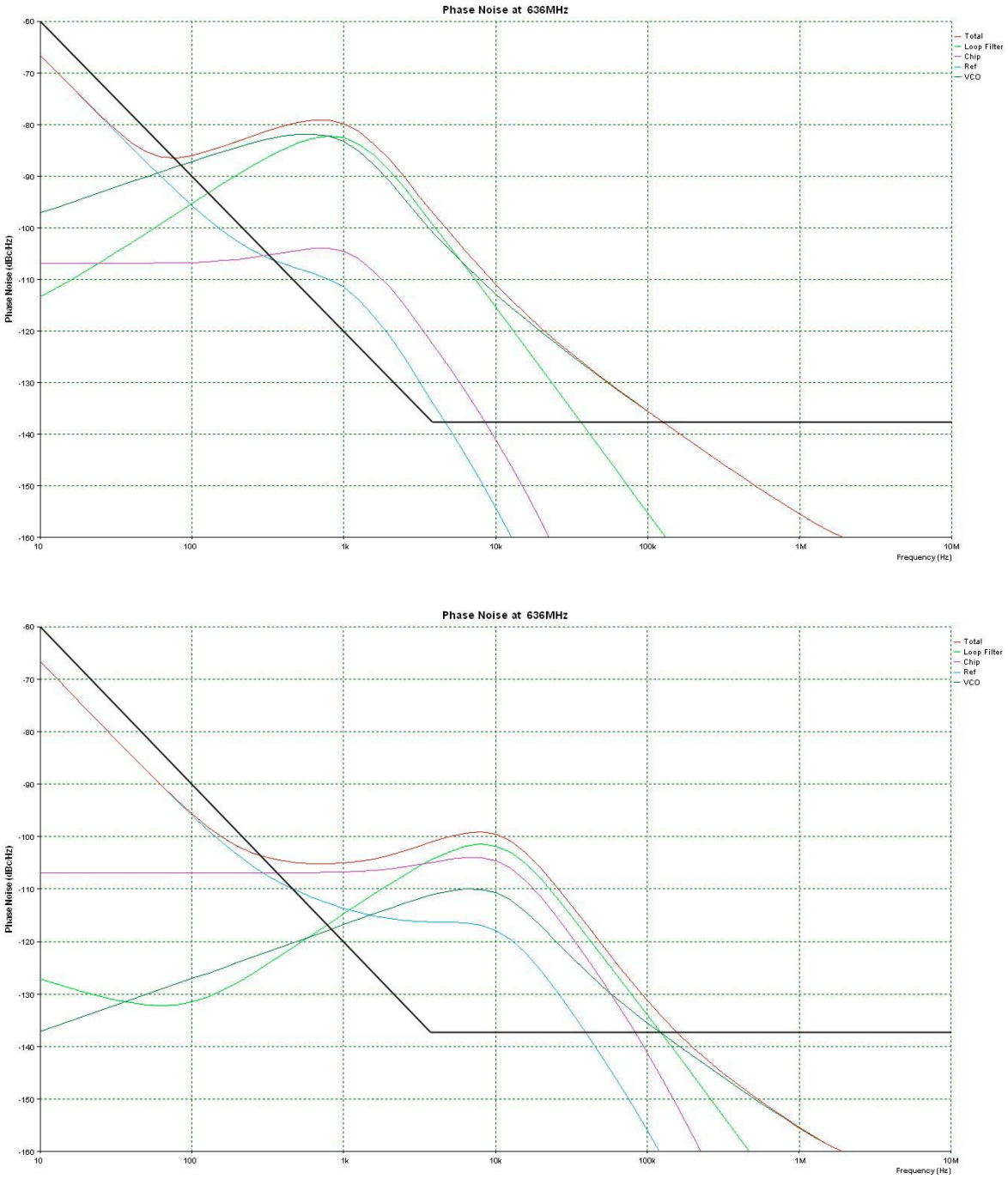

Figure 12 – VCXO/Multiplier (black) and VCO (color) Phase Noise

The VCXO/multiplier has an advantage between 80 Hz and 120 kHz or 300 Hz and 160 kHz depending on loop bandwidth. However, there is a degradation of 7 dB inside the text-mode carrier-recovery loop bandwidth and a degradation of up to 27 dB outside the passband of the receiver. The latter degradation is constant at 27 dB beyond 3 MHz and decreases the effectiveness of the SAW filters in the receiver over 80% of the PAVE PAWS frequency range.

If the external reference disappears or goes off frequency, each PLXO will stay within ±20 PPM of the correct frequency. This may cause the receiver to be off frequency by as much as 17 kHz or 8 kHz more than with a single common VCXO.

The first LO requires 2 stages of multiplication and the second LO requires 1 stage of multiplication. Each requires about 16 mW of RF power from MMIC amplifiers. 3 amplifiers at 40 mA total 120 mA. The VCXOs draw half the current of the VCOs, or 35 mA, and the common VCXO and PLL are eliminated, for a reduction of 10 mA. The additional current drain is then 75 mA from the 7 volt switching regulator or 570 mW assuming 90% regulator efficiency.

4. Conclusions

The delta-sigma PLL provides the safest approach as it eliminates any flash or EPROM memory on the receiver PCB.

If we trust flash memory, the integer-N PLLs can be used with a significant cost savings as long as the commercial versions survive radiation testing. If not, the rad-hard delta-sigma PLLs should be only slightly more expensive than rad-hard integer-N PLLs.

The VCXO/multiplier scheme provides no advantage for the additional power consumed.