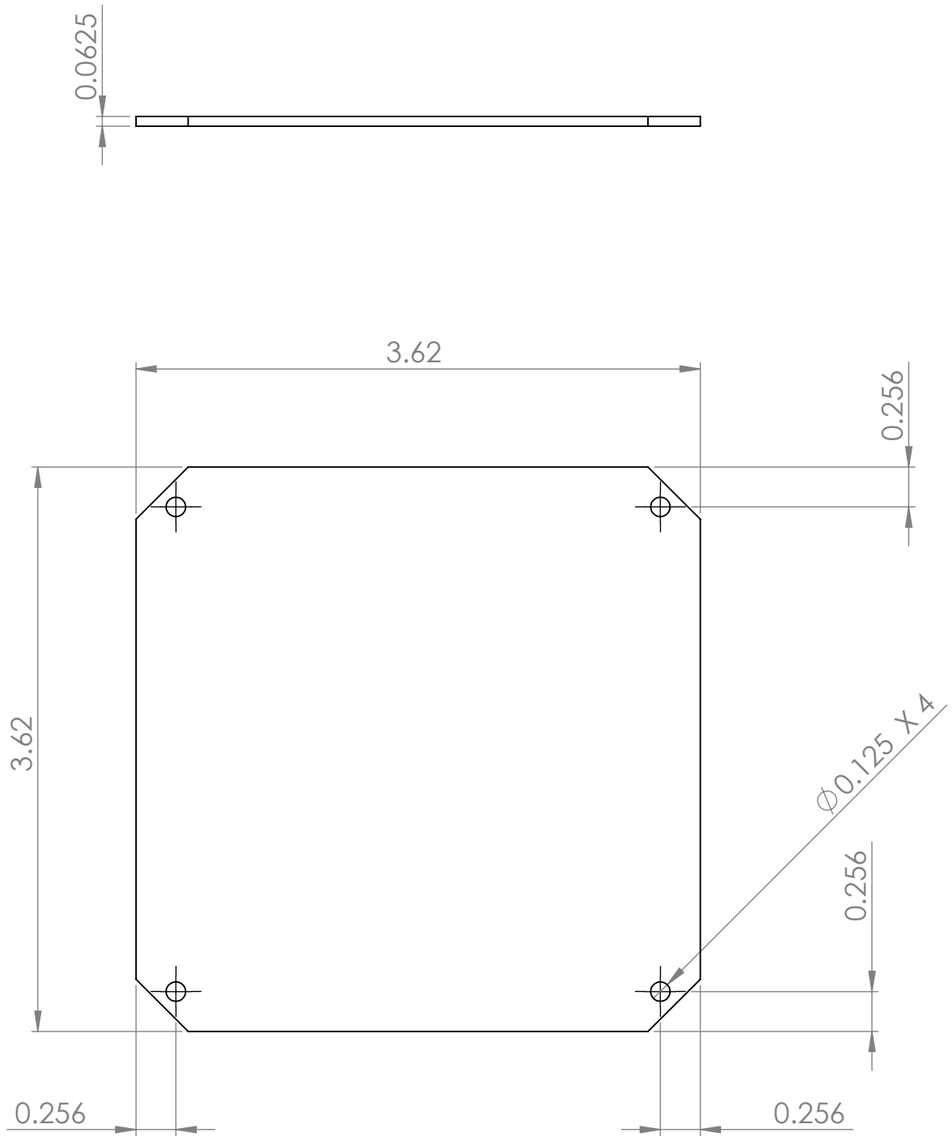
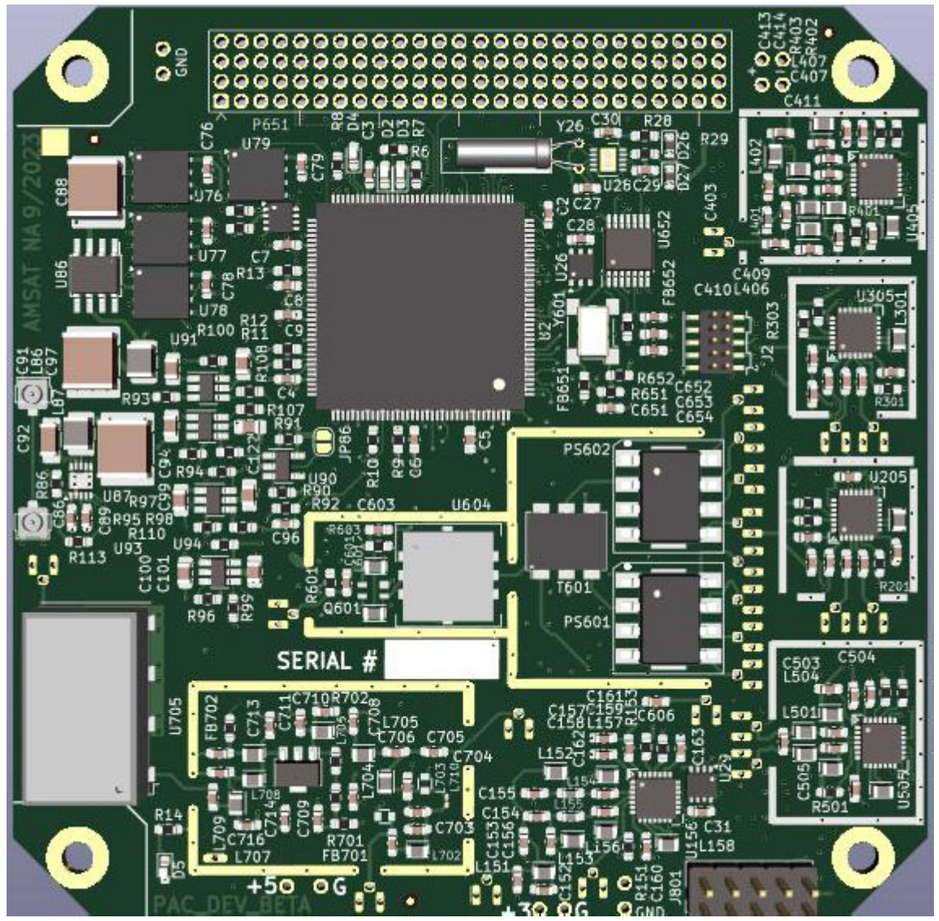
LAYOUT NOTES:
1) 6 Layer board.
2) Use standard FR-4 material
3) Goal is to have 5% Impedance tolarance but TBD
4) Employ lead free processing



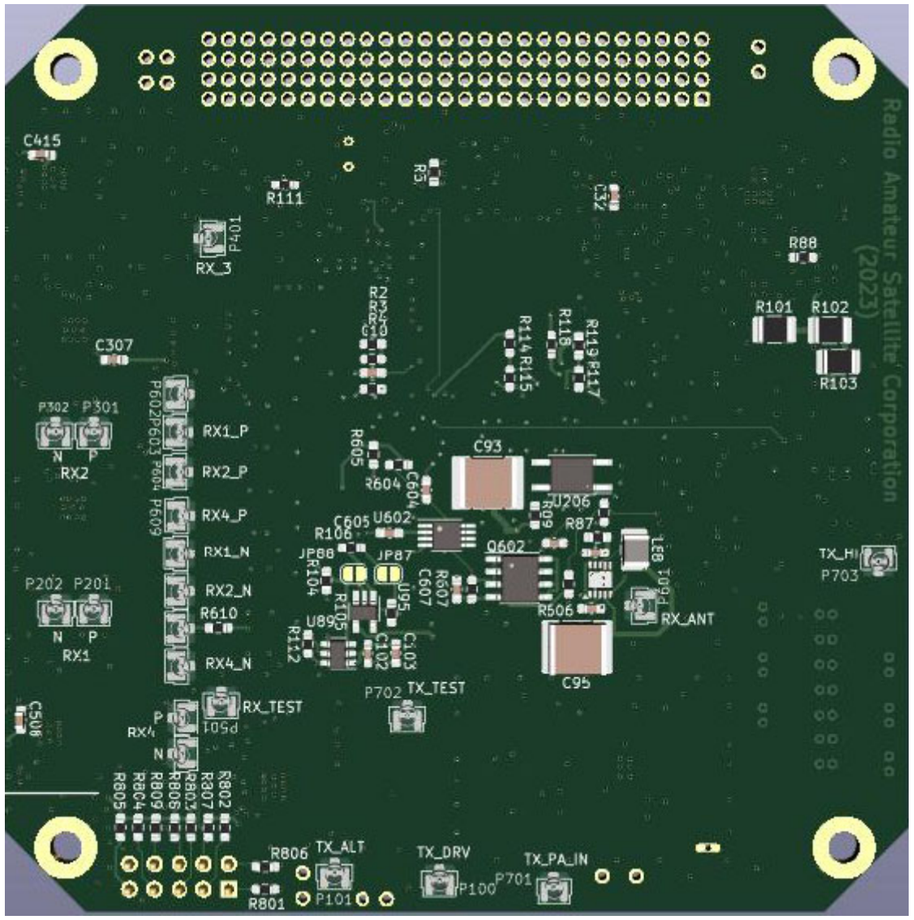
For Reference Only:

Propose PCB Stack Up					50 Ohms		
Layer	Type	Thickness (mil)			Trace width	Ref. layers	Calculated impedance
Top side solder mask			0.8	mils			
L1		copper+plating	1.4	mils	13mils	L2	50.83
			8	mils			
L2		copper	1.4	mils			
			5	mils			
L3		copper	1.4	mils			
			27.55	mils			
L4		copper	1.4	mils			
			5	mils			
L5		copper	1.4	mils			
			8	mils			
L6		copper+plating	1.4	mils	13mils	L5	50.83
Bottom side solder mask			0.8	mils			
TOTAL			63.55	mils			
			1.61	mm			

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN MILLIMETERS SURFACE FINISH: TOLERANCES: LINEAR: ANGULAR:	FINISH: Hot Air Solder Reflow				DEBUR AND BREAK SHARP EDGES	DO NOT SCALE DRAWING	REVISION
	NAME	SIGNATURE	DATE			TITLE: PacSat Dev PCB	
DRAWN	RSS N5BRG		230927				
CHK'D							
APPV'D							
MFG							
Q.A				MATERIAL: FR4		DWG NO. RSS2023092701	A3
				WEIGHT:		SCALE:1:1	SHEET 1 OF 2



Top Side



Bottom Side

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN MILLIMETERS SURFACE FINISH: TOLERANCES: LINEAR: ANGULAR:		FINISH:			DEBUR AND BREAK SHARP EDGES	DO NOT SCALE DRAWING	REVISION
	NAME	SIGNATURE	DATE			TITLE: PacSat Dev PCB	
DRAWN	RSS N5BRG		230927				
CHK'D							
APPV'D							
MFG							
Q.A				MATERIAL: FR4		DWG NO. RSS2023092701	A3
				WEIGHT:		SCALE:1:1	SHEET 2 OF 2